Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A calculation unit ~~mathematical engine~~ comprising:

a parallel output shift register receiving data to be processed; ~~and~~

a processor configured with a predetermined capacity for processing data vector elements and including an adder tree using a plurality of arithmetic logic unit (ALU) circuits, ~~for accepting~~ the processor configured to accept the output of the shift register and ~~for providing~~ to provide a data output; and

~~whereby~~ the shift register ~~includes~~ configured with a selectable initial position for a data vector which exceeds the capacity of the processor so as to selectively output the data based upon the capacity of the processor.

2. (Currently Amended) The calculation unit ~~mathematical engine~~ of claim 1, further comprising a multiplexer configured to receive selectively~~, for receiving an~~ output data from the parallel output shift register and ~~providing~~ to selectively provide such data from the parallel output shift register as input to the processor ALU circuits.

3. (Currently Amended) The calculation unit ~~mathematical engine~~ of claim 2 wherein the parallel output shift register has both serial and parallel inputs further characterized by an ~~comprising at least one~~ enable circuit~~,~~ configured to selectively enable ~~the output from~~ the shift register serial and parallel inputs.

4. (Currently Amended) The calculation unit ~~mathematical engine~~ of claim 1, wherein said processor is configured to process data that includes both real and imaginary components.

5. (Currently Amended) A calculation unit for performing a plurality of different types of calculations, the calculation unit comprising:

at least one input memory for storing data;

a parallel output shift register;

a multiplexer, for receiving the output from said shift register and providing an output to an adder tree;

the adder tree comprising a plurality of arithmetic logic units (ALUs); and

a selection circuit for selectively enabling the shift register, ~~and~~ the multiplexer and the at least one input memory to apply certain portions of the input data to the adder tree based on the type of calculation performed~~, to perform different calculations~~.

6. (Original) The calculation unit of claim 5, further comprising, at least one selectable memory having a data width of at least a multiple of a data width of the adder tree.

7. (Currently Amended) The calculation unit of claim 1 wherein the parallel output shift register is configured as ~~A mathematical engine for performing calculations, the mathematical engine including: at least one input memory for storing input data;~~ a selectable memory for receiving ~~the~~ input data from ~~said~~ at least one input source ~~memory~~ and ~~for~~ the shift register is configured to provide ~~providing~~ a selectable output via a plurality of folds, wherein each said fold comprises at least one different position within the selectable memory~~; and a~~

~~processor array having a plurality of processors for receiving an output from the selectable memory and selectively providing an output~~.

8. (Currently Amended) The calculation unit ~~mathematical engine~~ of claim 7, further comprising an input memory configured to serve as said at least one input source and an enablement circuit to selectively control said ~~at least one~~ input memory and said selectable memory depending upon the desired mathematical calculation.

9. (Currently Amended) The calculation unit ~~mathematical engine~~ of claim 8, further including ~~an adder tree, having a plurality of arithmetic logic unit circuits, for receiving an output from the processor array and for processing the output; and~~ an accumulation circuit for receiving and selectively accumulating each output from the adder tree based on the type of calculation performed~~; whereby said enablement circuit further controls at least a portion of the adder tree, support the desired mathematical calculation~~.

10. (Currently Amended) The calculation unit of claim 1 further ~~A computation circuit for resolving complex functions; the computation circuit~~ comprising:

a memory~~, for receiving~~ configured to receive input data for complex resolution;

a store~~, for storing~~ configured to store an operational factor for ~~the~~ a complex function;

a multiplexer~~, for receiving an~~ configured to selectively receive input from the parallel output shift register via the memory ~~and the operational factor~~ or the store;

the processor ALU circuits configured as a processing array circuit, for processing data from selected ~~according to a number of~~ bit locations stored by the memory~~, the processing array circuit including an~~ and data output from the multiplexer ~~and at least some of the input data; a complex adder tree receiving outputs from the processing array and providing an added output~~; and

an accumulator circuit ~~receiving~~ configured to receive an output from the adder tree and ~~providing~~ to provide an accumulated complex output.

11. (Cancelled)

12. (Currently Amended) The calculation unit ~~computation circuit~~ of claim 10~~, further comprising providing~~ the store is configured to provide a twiddle factor as the operational factor, for performing discrete Fourier transforms (DFTs), wherein the multiplexer receives its input from the store when using the twidde factor ~~memory and the operational factor~~.

13.-18. (Cancelled)

19. (New) A communication device including the calculation unit of claim 1 configured to facilitate processing of wireless communication signals.

20. (New) A communication device including the calculation unit of claim 5 configured to facilitate processing of wireless communication signals.

21. (New) A communication device including the calculation unit of claim 7 configured to facilitate processing of wireless communication signals.

22. (New) A communication device including the calculation unit of claim 10 configured to facilitate processing of wireless communication signals.

23. (New) A method of processing wireless communication signal data using a parallel output shift register that receives data to be processed and a processor that includes an adder tree associated with a plurality of arithmetic logic unit (ALU) circuits that define a processor capacity characterized by selectively controlling the shift register to selectively output data based upon the capacity of the processor and using the processor to process output of the shift register and to provide a processed.

24. (New) The method of claim 23 further comprising using a multiplexer to receive selectively output data from the parallel output shift register and to selectively provide such data from the parallel output shift register to the processor ALU circuits.

25. (New) The method of claim 24 wherein the parallel output shift register has both serial and parallel inputs further comprising selectively enabling the shift register serial and parallel inputs based on the type of data processing computations to be performed.

26. (New) The method of claim 25 wherein an input memory is associated with the parallel output shift register and the processor ALU circuits, further comprising selectively enabling input to the shift register and the processor ALU circuits from the input memory based on the type of calculation performed.

27. (New) The method claim 26 further comprising selectively enabling input from a secondary input memory to the processor based on the type of calculation performed.

28. (New) The method of claim 27 wherein the data which is processed is data that includes both real and imaginary components.